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MS-7817

mATX

Ver: 12

Intel Sharkbay plamform H81

CPU:

INTEL-Haswell LGA1150

System Chipset:

INTEL-LYNX

Memory:

DDRIII (1333/1666MHz) * 2 (Dual Channel)

PWM:

VRD12 - ISL95812

OnBoard Chipset:

HD Audio Codec:RTL892

LAN-realtek8111G

SIO:NUVOTON 5533D

SPI ROM: 64 MB

Other:

DVI*1

VGA*1

SATA2*2

SATA3*2

FRONT USB2.0 *2

REAL USB2.0 *4

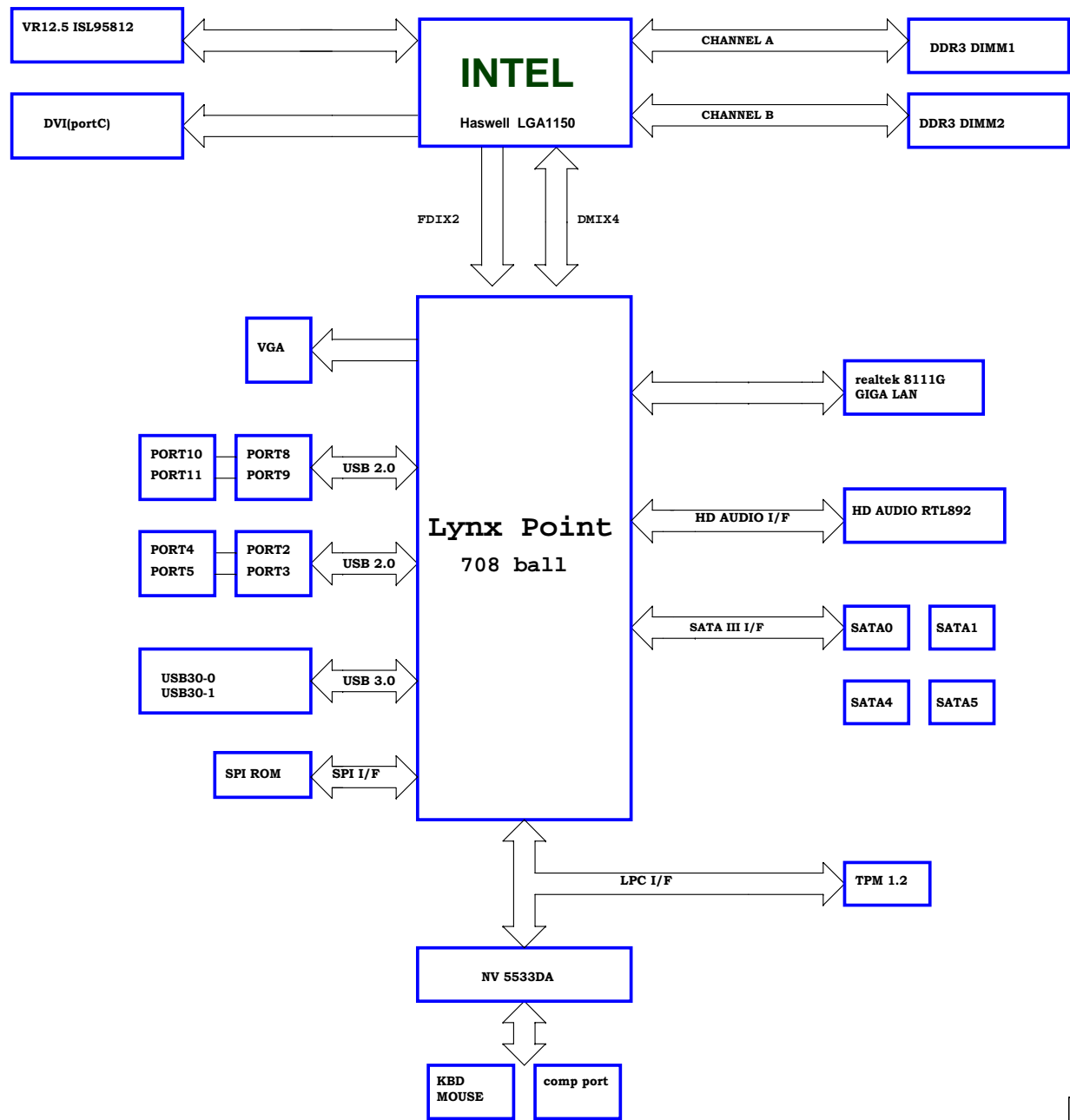
REAL USB3.0 *2

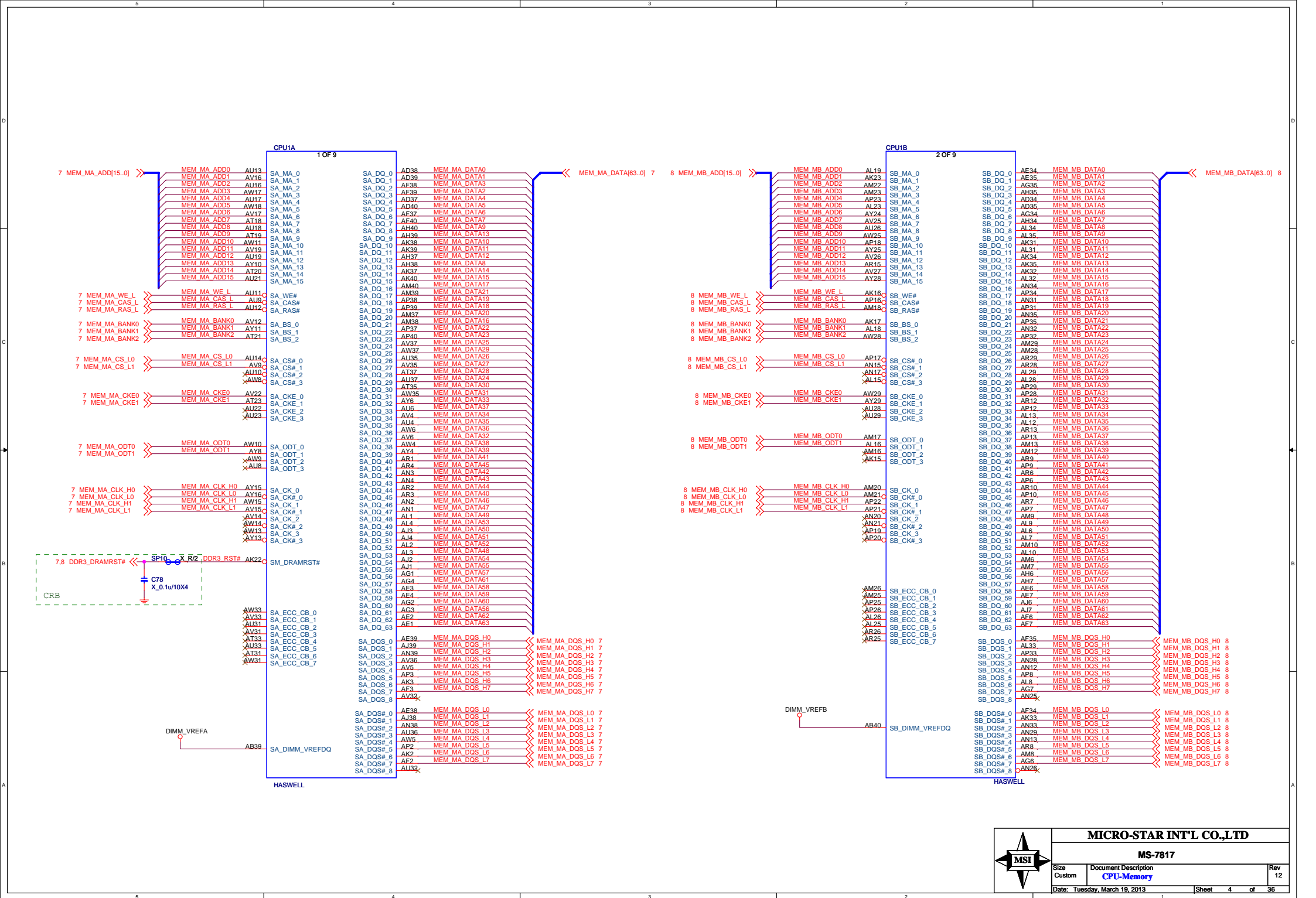
Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 1

MS-7817 Block Diagram





GND

GND

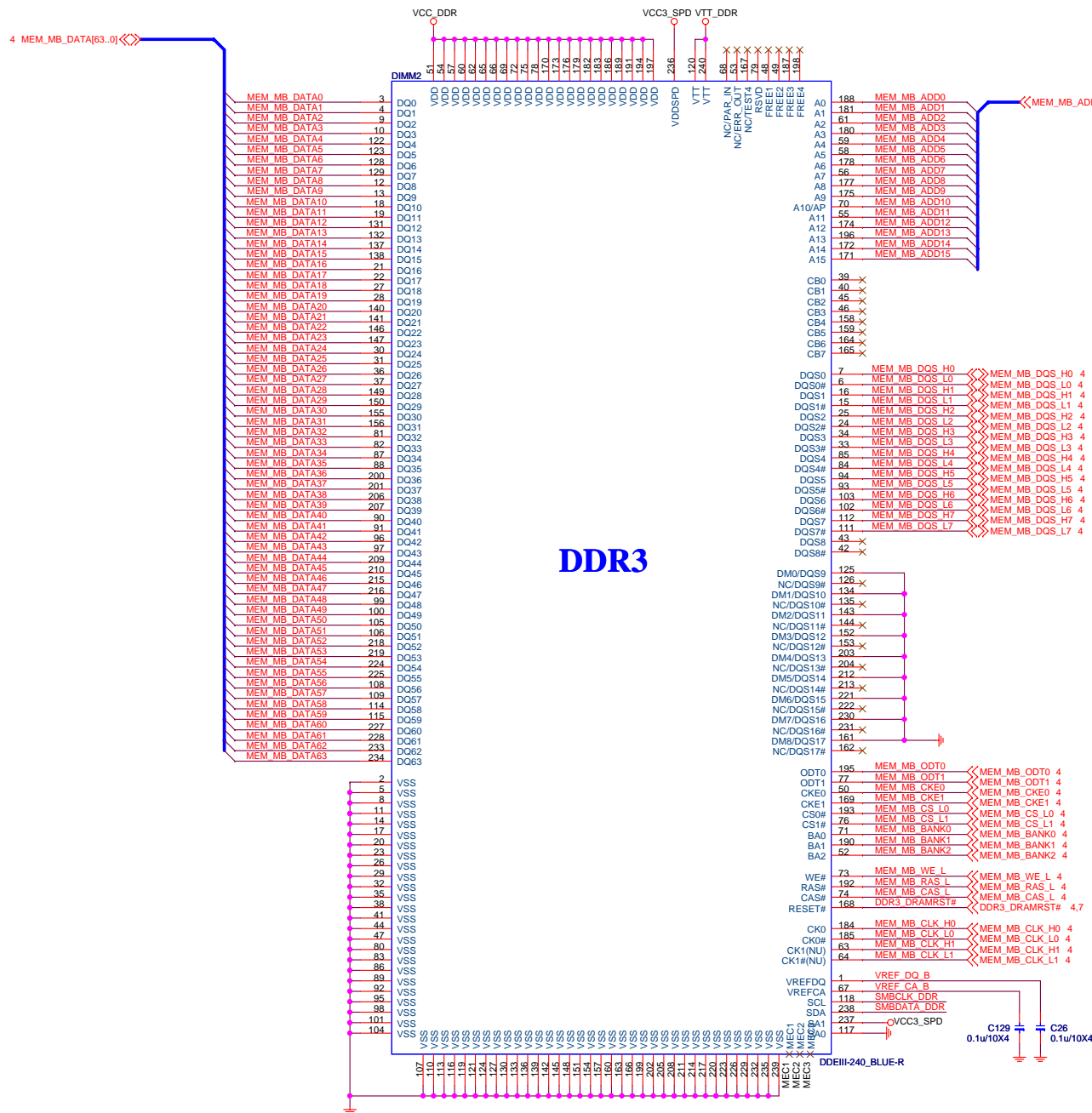


MICRO-STAR INT'L CO.,LTD

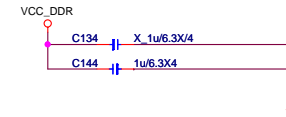
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|-------------------------------|----------------------|---------------|
| Custom | CPU-GND | 12 |
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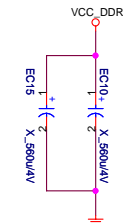
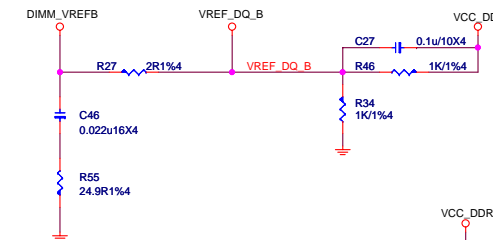
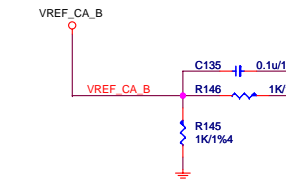
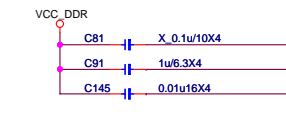
DDRIII DIMM_B0



Place close to DIMM2



Place close to DIMM2

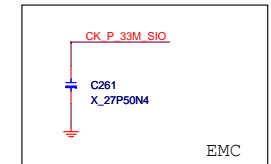


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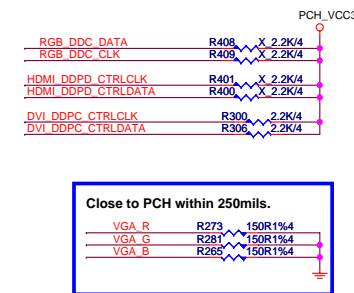
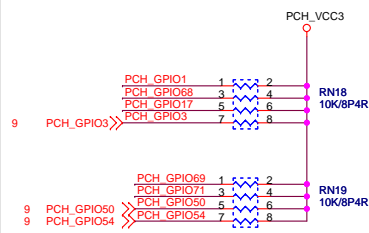
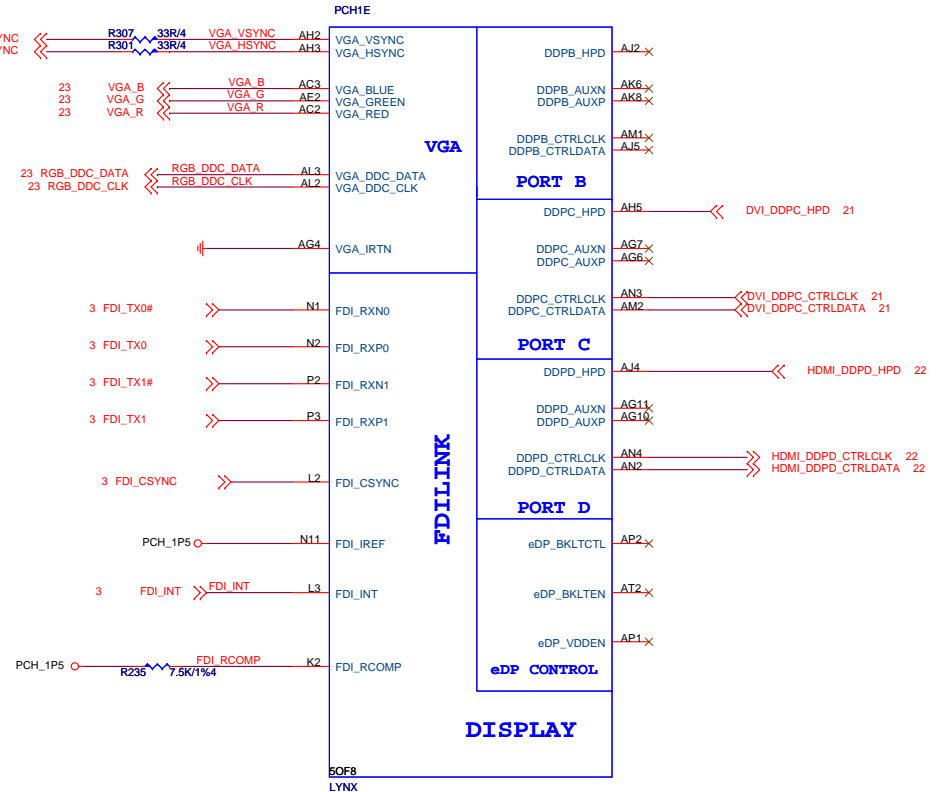
| | | |
|-------------------------------|--|---------------|
| Size Custom | Document Description DDR3 Chanel-B DIMM3/4 | Rev 12 |
| Date: Tuesday, March 19, 2013 | | Sheet 8 of 36 |


```
pcie port7,8 NA
```



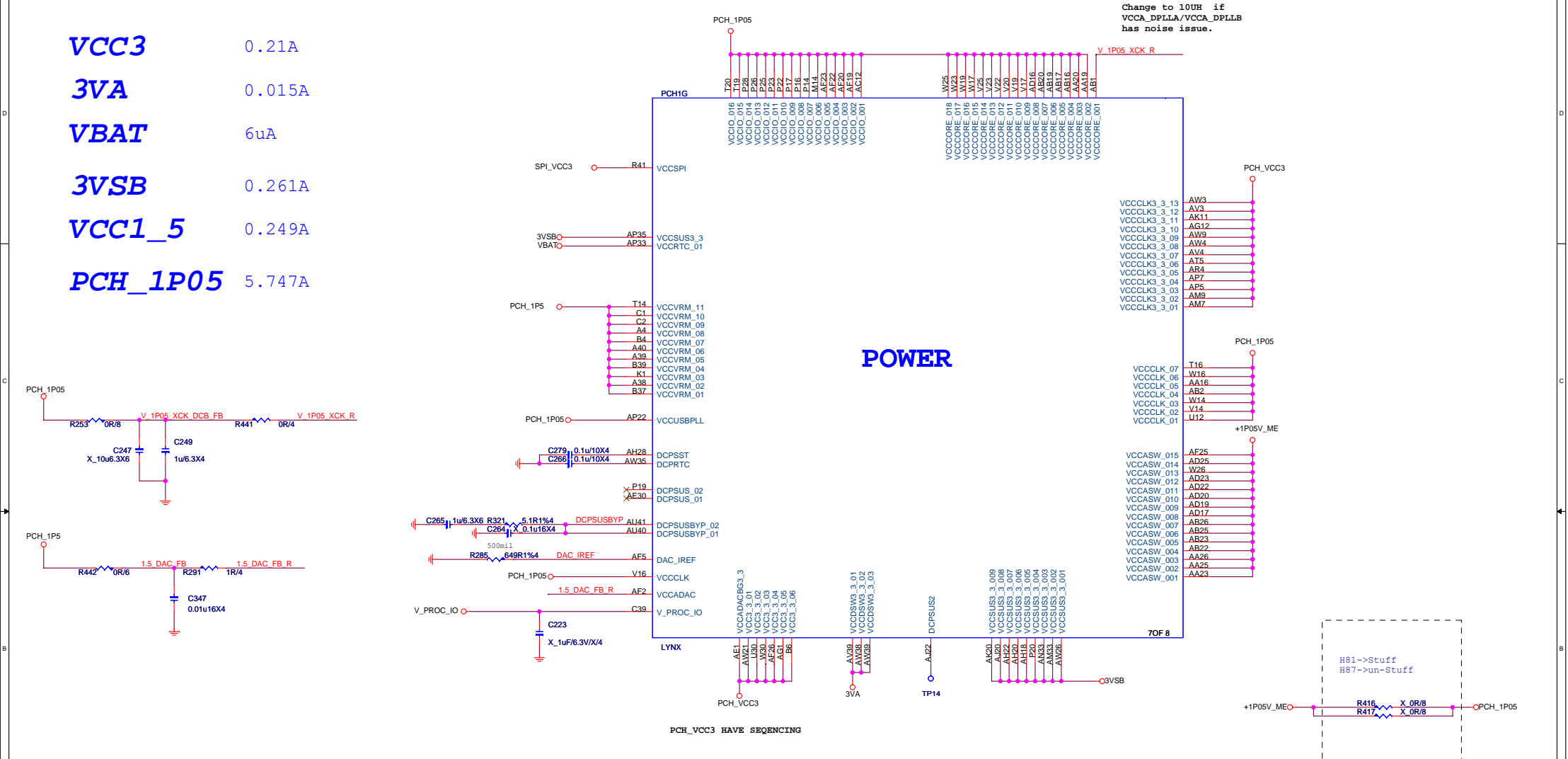
| | | |
|-------------------------------|---|---------------|
| Size Custom | Document Description PPT PCIE/DMI/USB/CLK | Rev 12 |
| Date: Tuesday, March 19, 2013 | | Sheet 9 of 36 |

SATA 6 Gb/s support on ports 0 and 1 only.

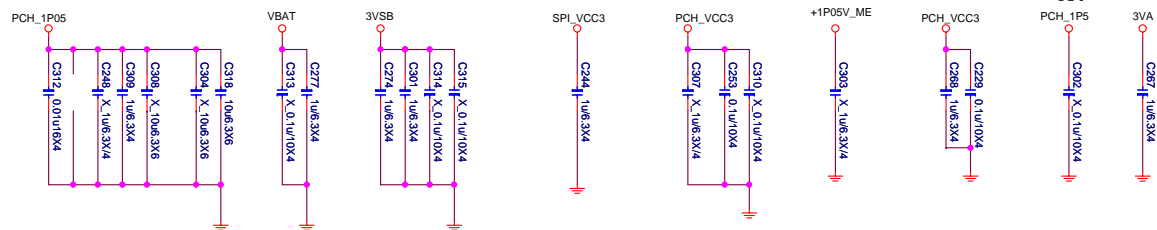
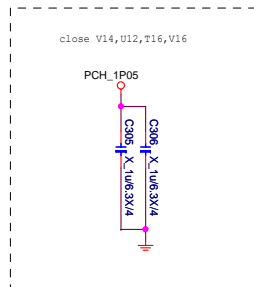


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|-------------------------------|---|----------------|
| Size Custom | Document Description PPT SATA/HOST/FAN/GPIO/VGA | Rev 12 |
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| | |
|------------------------|--------|
| <i>VCC3</i> | 0.21A |
| <i>3VA</i> | 0.015A |
| <i>VBAT</i> | 6uA |
| <i>3VSB</i> | 0.261A |
| <i>VCC1_5</i> | 0.249A |
| <i>PCH_1P05</i> | 5.747A |



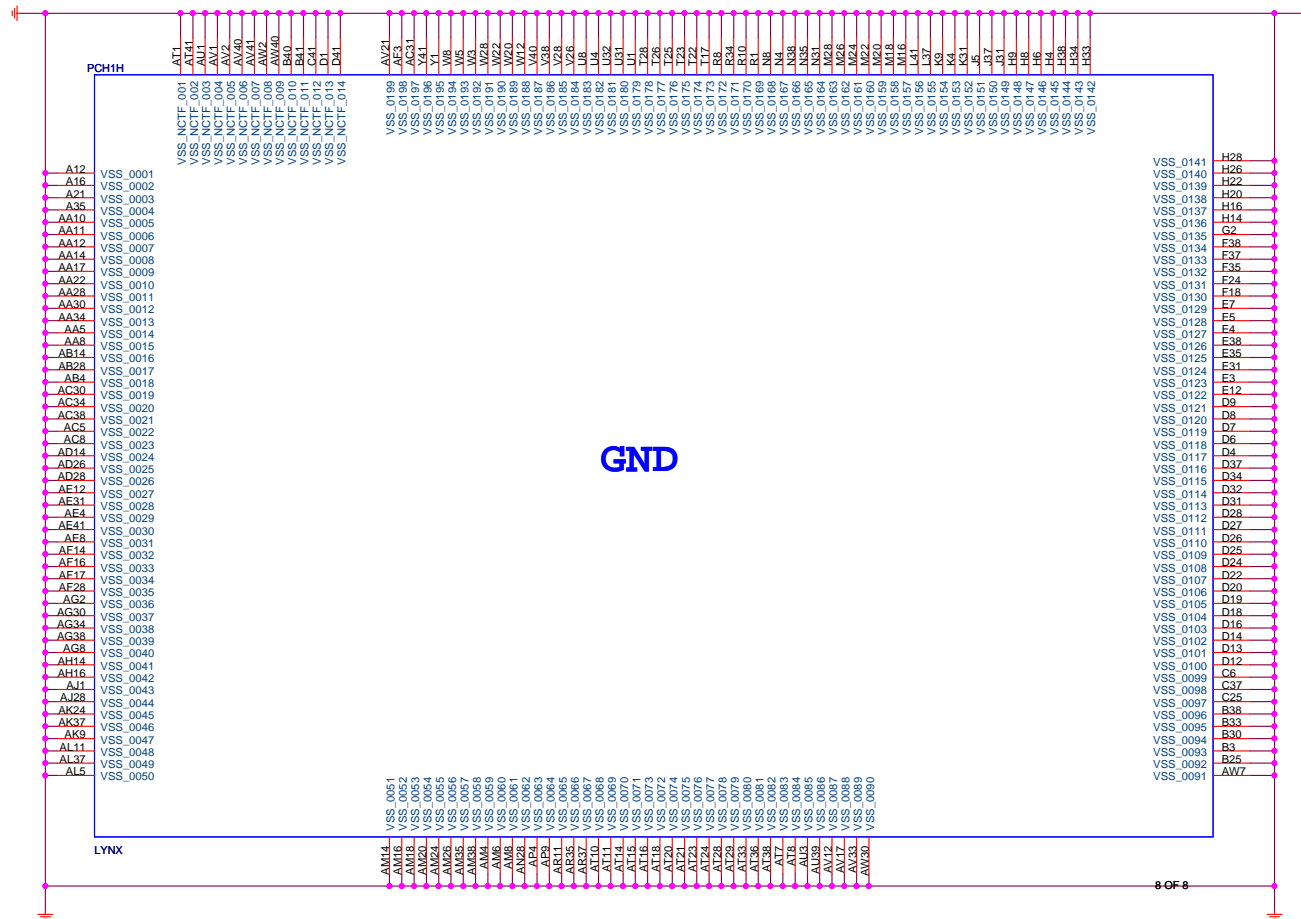
PCH decoupling cap



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| | | |
|-------------------------------|---|----------------|
| Size Custom | Document Description LYNX-POWER PIN | Rev 12 |
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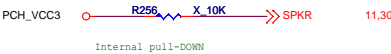


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|-------------------------------|--|----------------|
| Size Custom | Document Description PPT GND/NVRAM | Rev 12 |
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PCH Straps

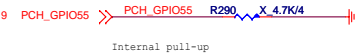


SPKR

Default Mode:

Internal weak Pull-down.

No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



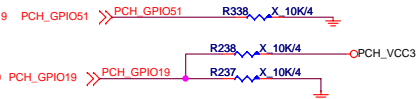
GPIO55

Default Mode:

Internal pull-up.

Top Block Swap Mode:

Connect to ground with 4.7k Ohm weak pulldown resistor.



SATA1GF/GPIO19, GPIO51

Default (SPI):

Left both SATA1GF/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:

Connect SATA1GF/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:

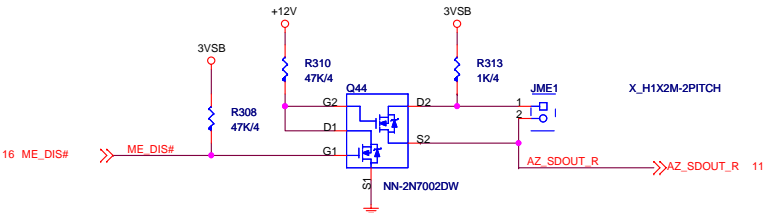
Connect both SATA1GF/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.



GPIO53

Do not pull low.

Connect to ground with 1k Ohm pull-down resistor.



HDA_SDO

Default:

Do not pull high.

Disable ME in Manufacturing Mode:

Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

GPIO37

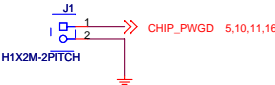
Enable TLS:

Pull up with 1k Ohm to VccSus3.3.

Default (Disable TLS):

Leave NC. Internal pull down.

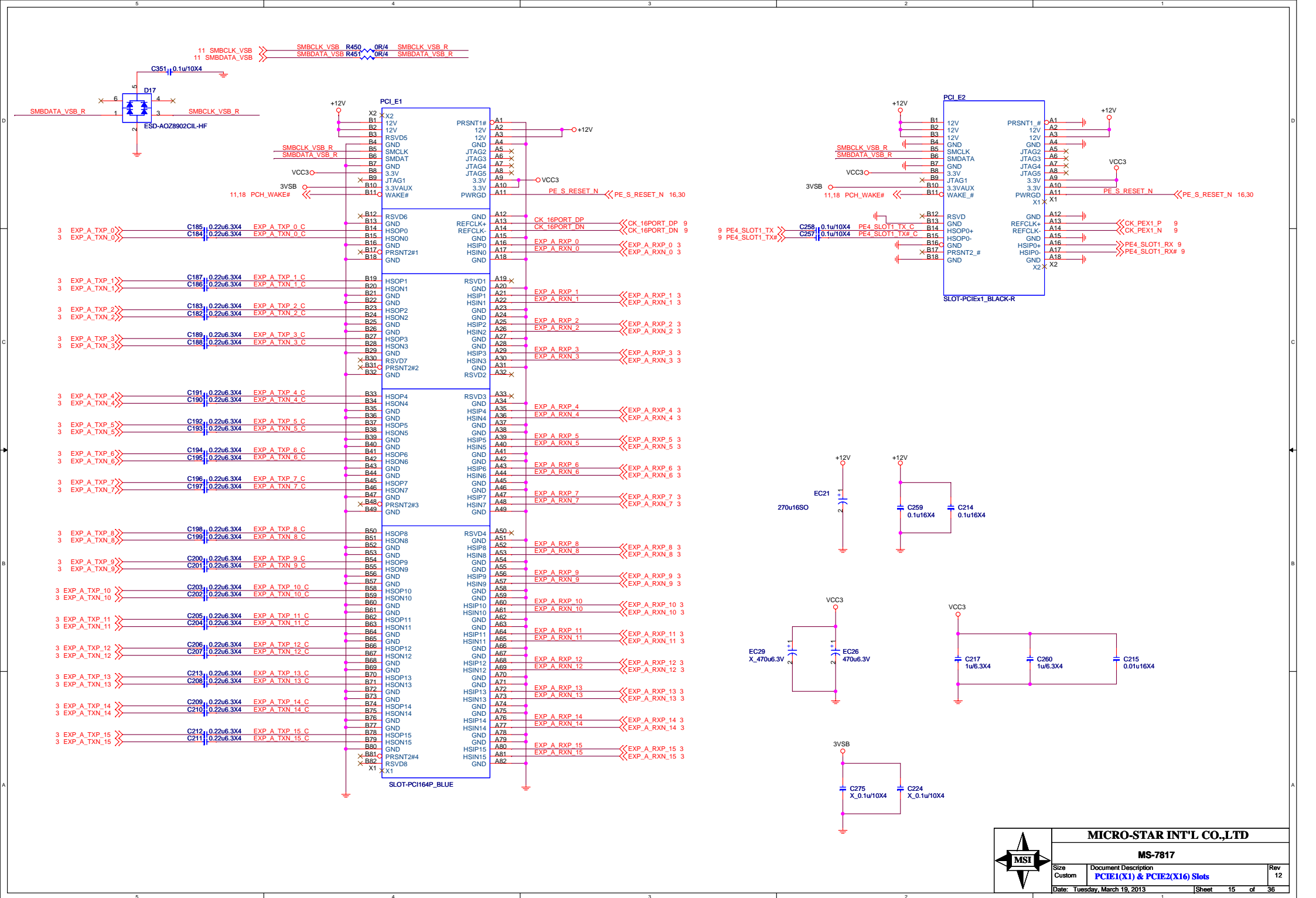
For test cpu voltage

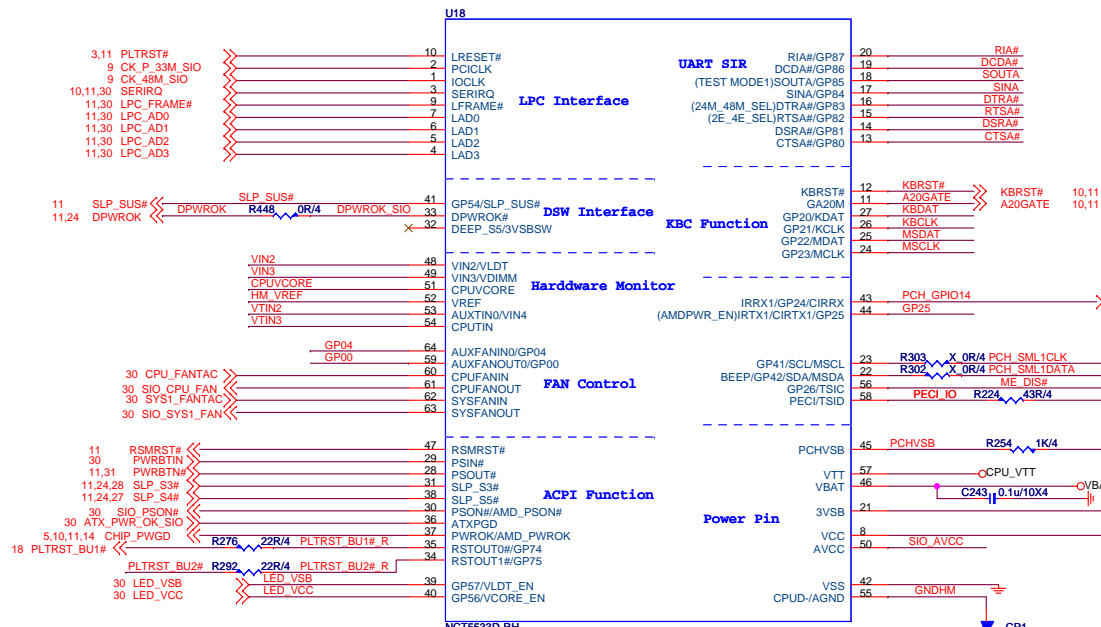


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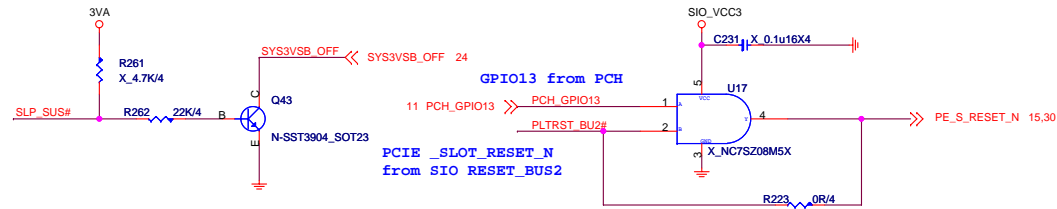
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|--------|-------------------------|----------------|
| Custom | PPT STRAPS | 12 |
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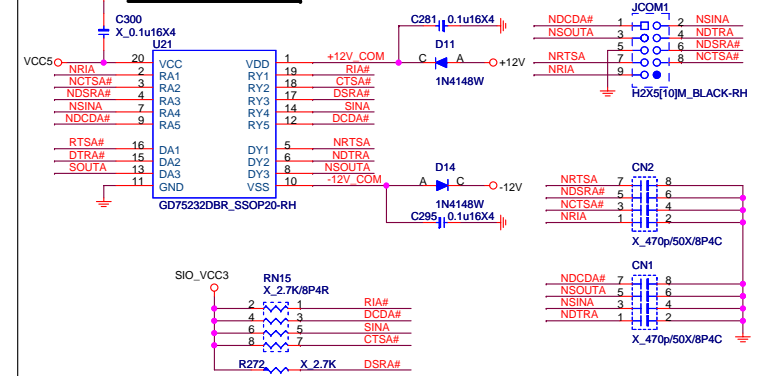




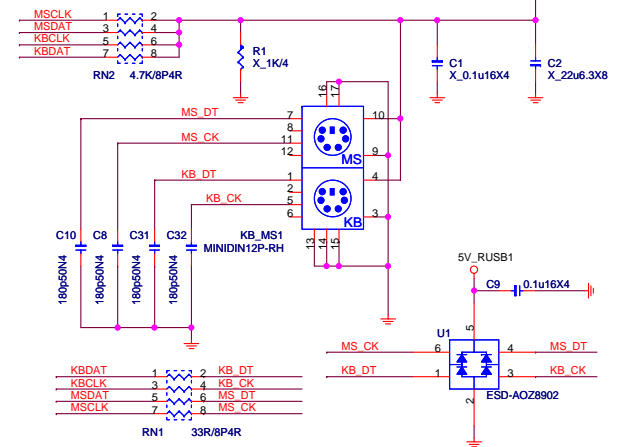
5533D DSW SUPPORT



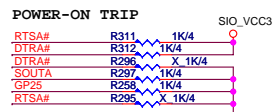
SERIAL PORT 1



PS2 Connector



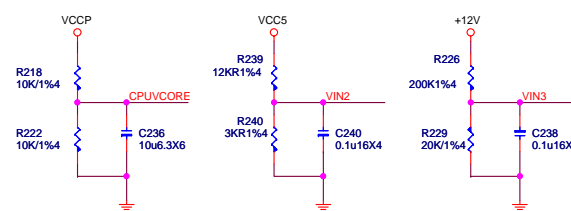
LPC I/O STRAPPING RESISTOR



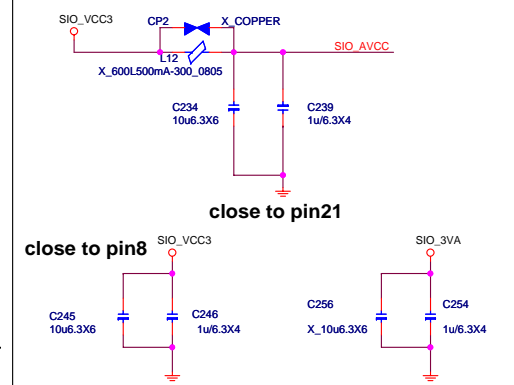
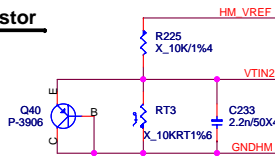
NCT5533D POWER ON STRAPPING PIN

| PIN | Function | NET Name | HI | LO |
|-----|-------------|----------|--------------------|---------------------|
| 44 | AMD_PWR_EN | | ENABLE AMD PWR SEQ | DISABLE AMD PWR SEQ |
| 18 | TEST_MODEL | SOUTA | TEST MODE 1 ENABLE | TEST MODE 1 DISABLE |
| 16 | 24M_48M_SEL | DTRA# | 48MHz | 24MHz |
| 15 | 2E_4E_SEL | RTSA# | 4E | 2E |

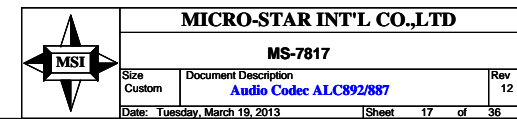
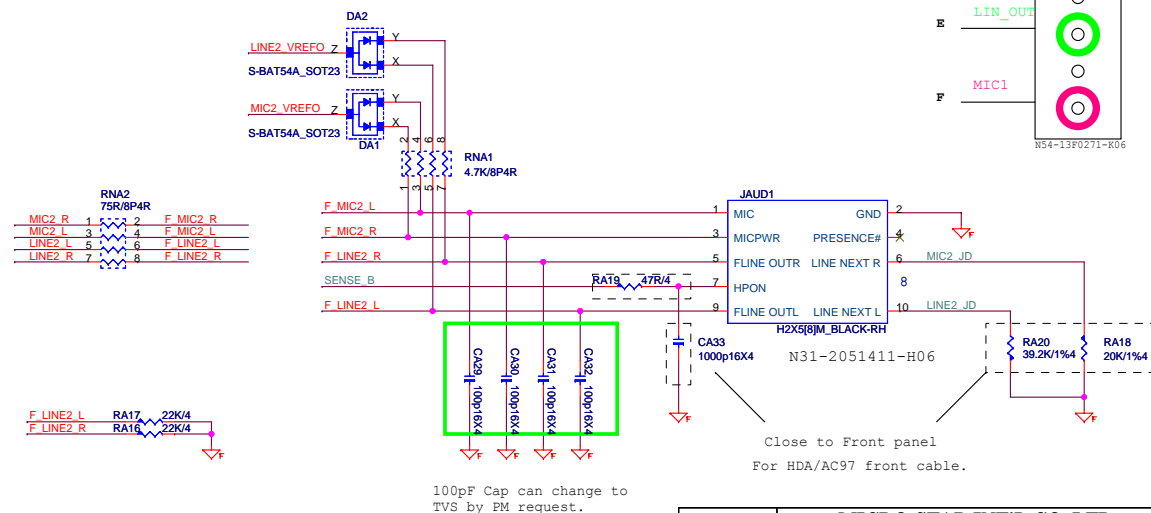
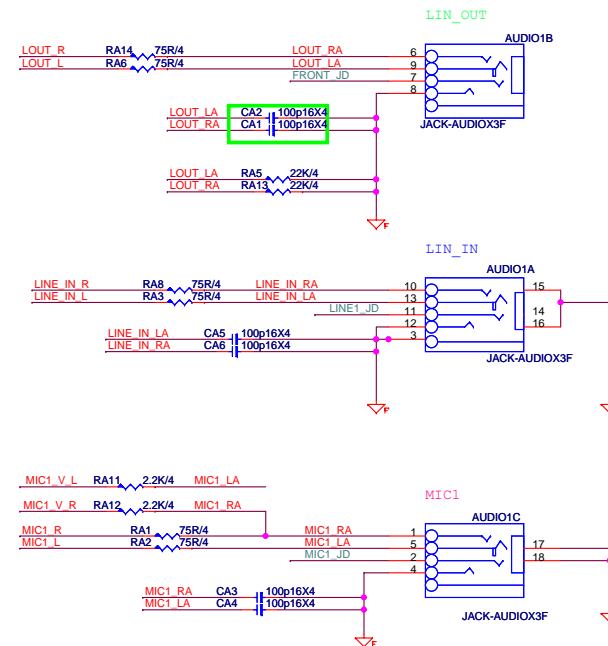
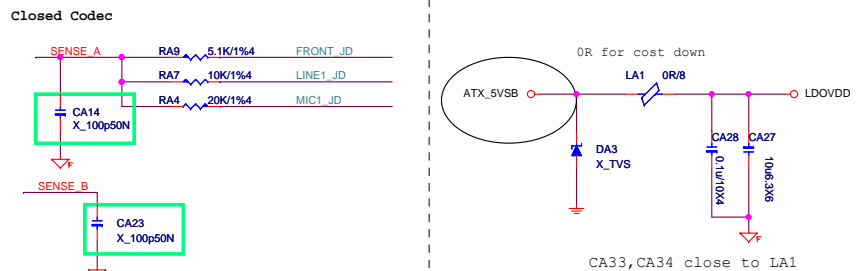
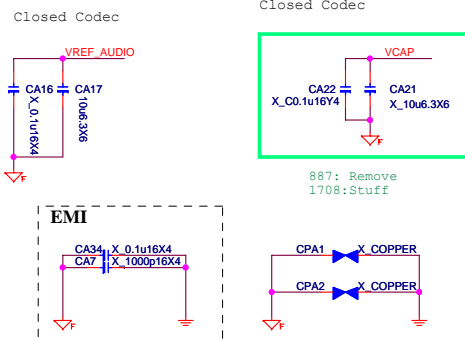
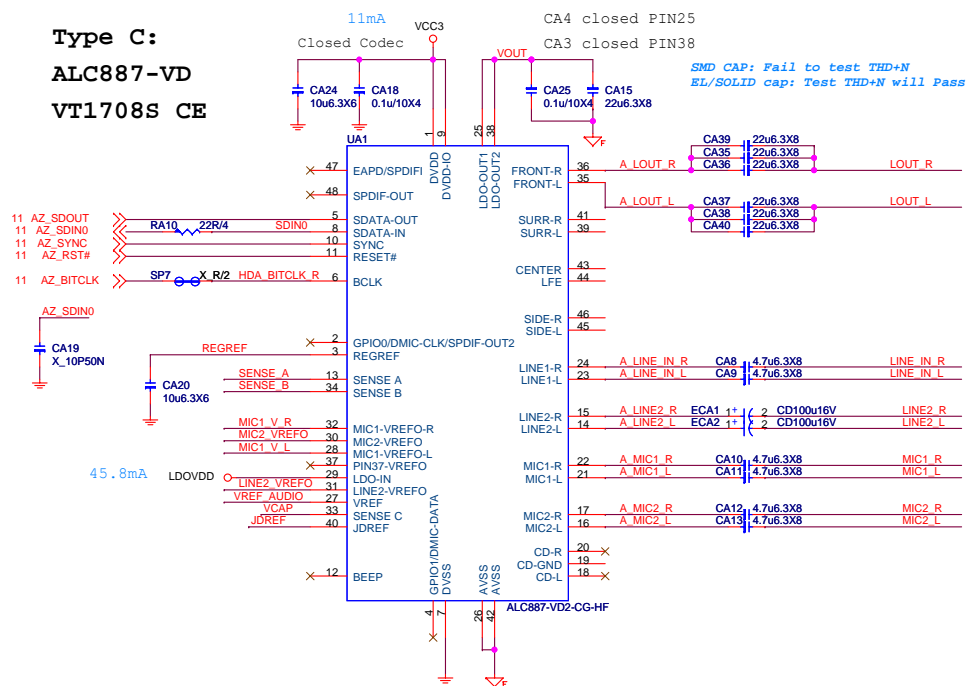
Voltage Sensing



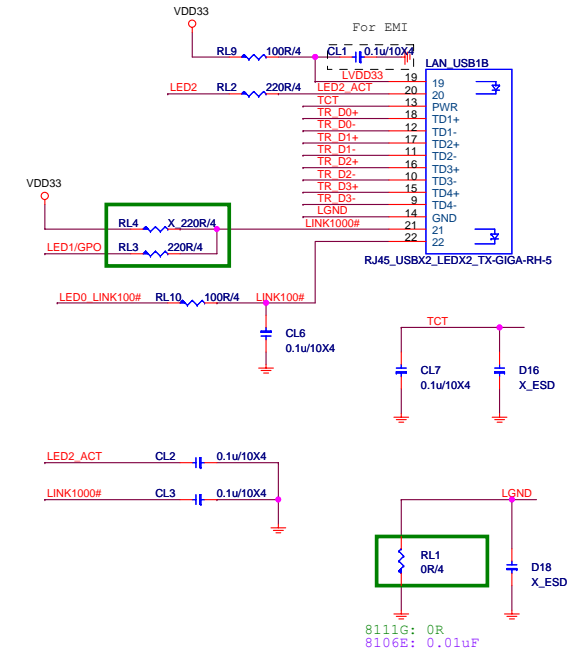
Thermal Resistor



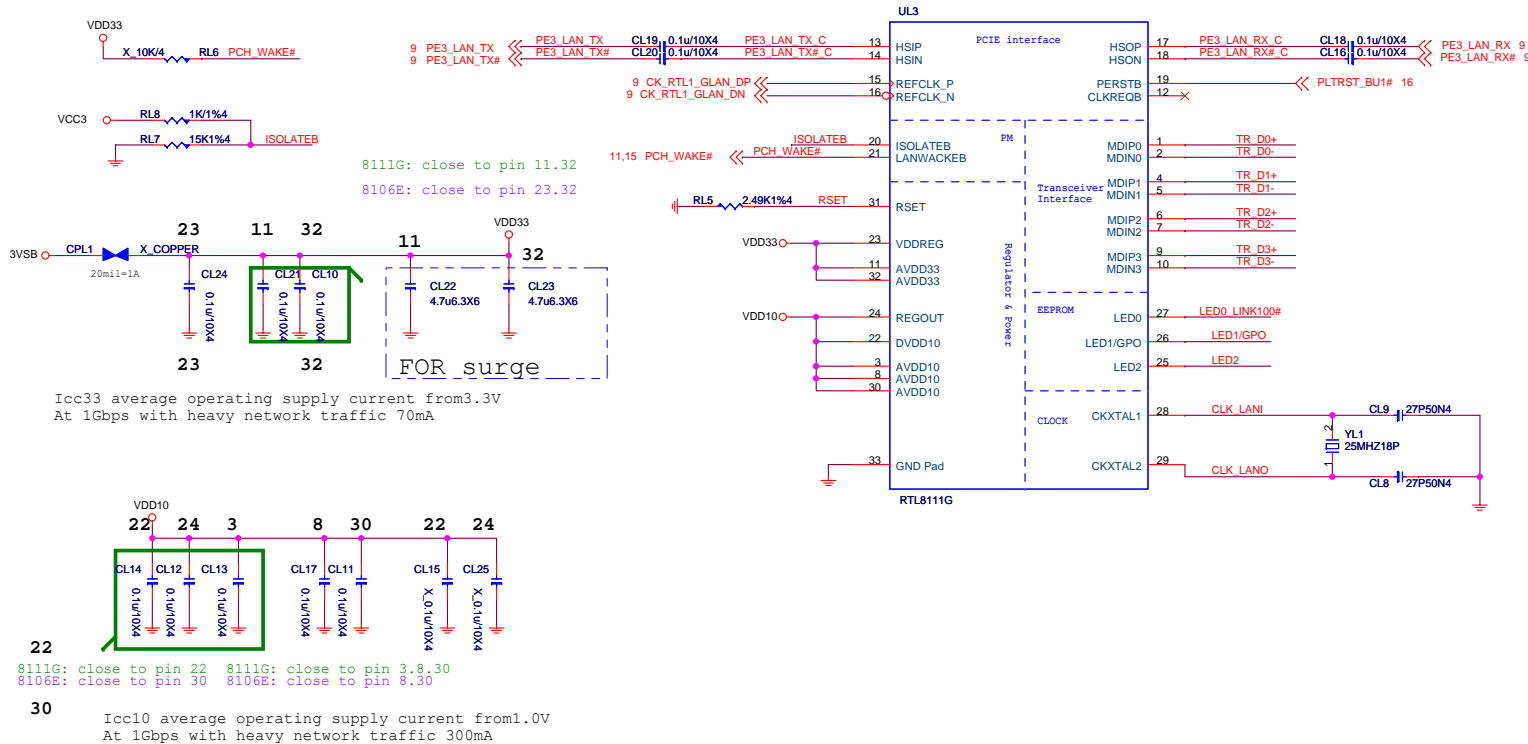
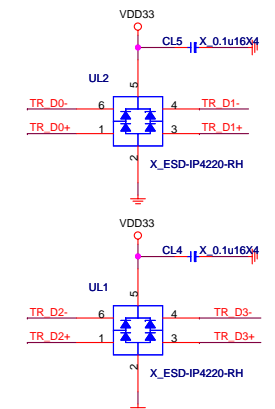
Type C:
ALC887-VD
VT1708S CE



```
RTL8111G Giga LAN
RTL8106E 10/100M LAN
```



Reserve ESD Protect

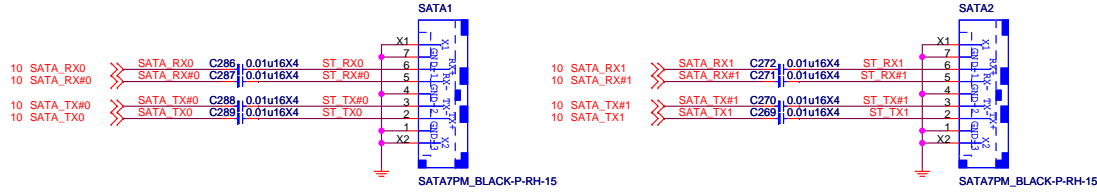


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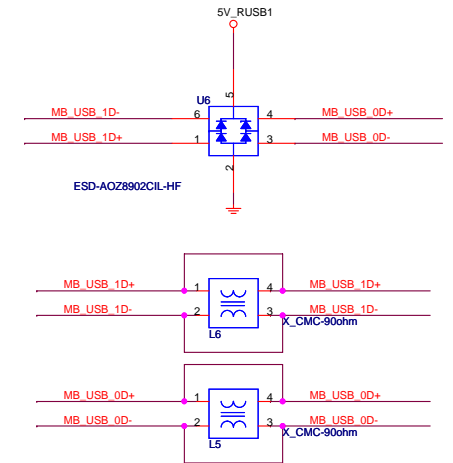
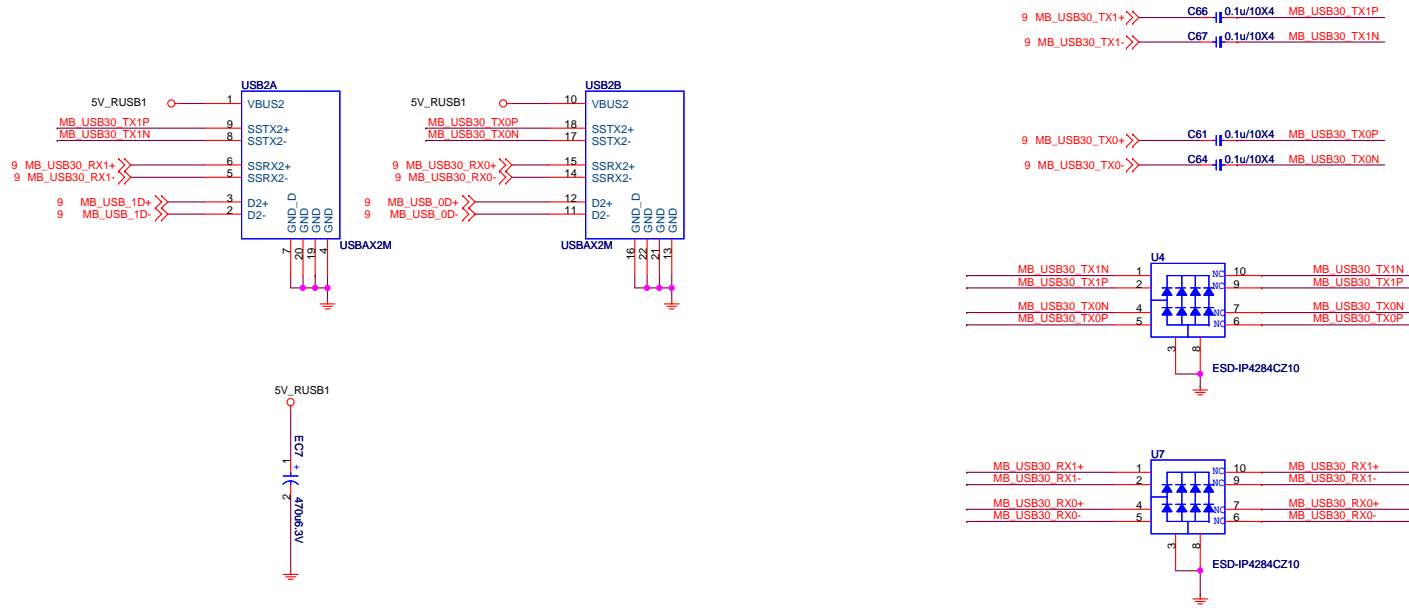
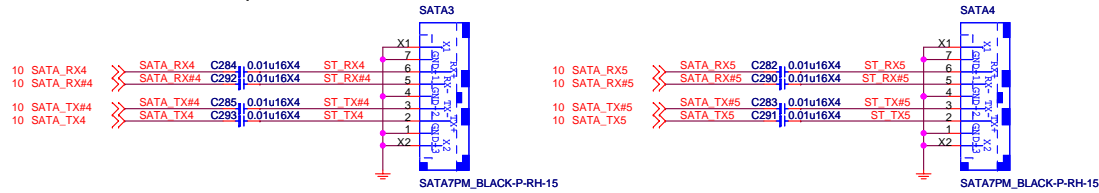
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|-------------------------------|---|----------------|
| Size Custom | Document Description LAN RTL8111G/8106E | Rev 12 |
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SATA 6G PORT 0,1



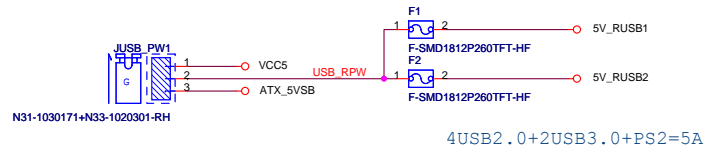
SATA 3G PORT 4,5



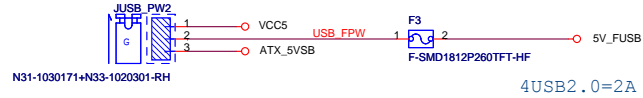
Type C: jumper +Fuse

PCH/FCH side: OC# pull high to +3VSB

Near Rear ==>



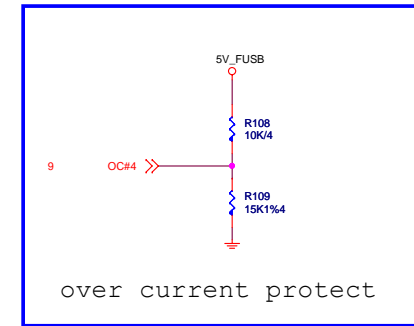
Near Front ==>



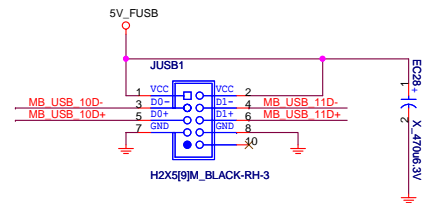
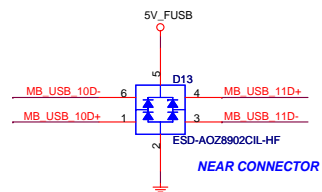
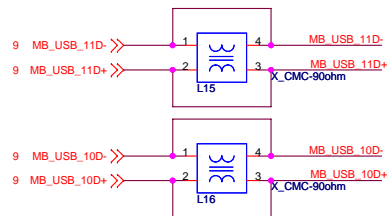
D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)
D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 usb 2.0 ports (1A)

Default VCC5 (PIN1-2)

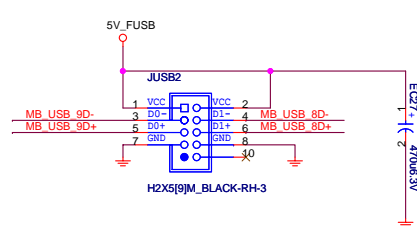
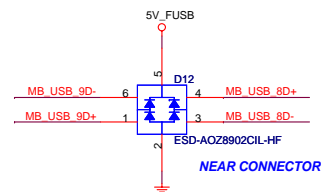
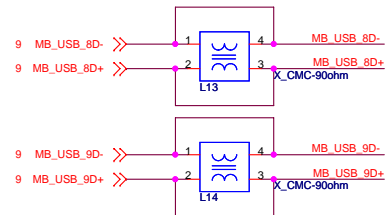
| JUSB_FW | BIOS Menu | Wake up support |
|---------|-------------|-----------------|
| 1-2 | EUP Enable | Not support |
| | EUP Disable | Not support |
| 2-3 | EUP Enable | Not support |
| | EUP Disable | support |



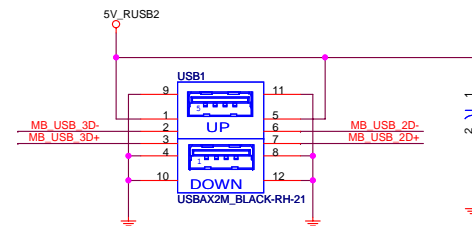
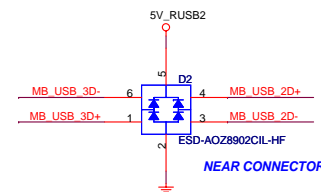
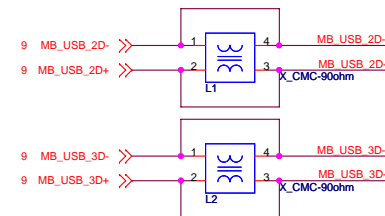
FRONT USB PORT 8,9



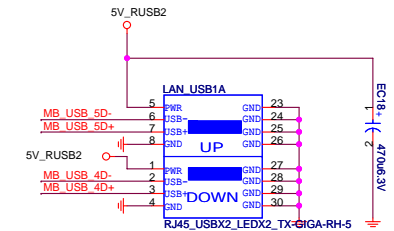
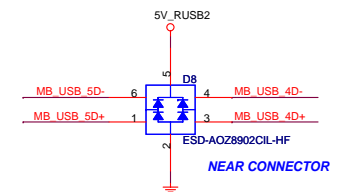
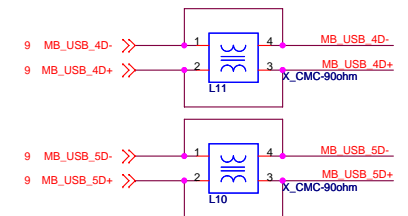
FRONT USB PORT 10,11



FRONT USB PORT 10,11

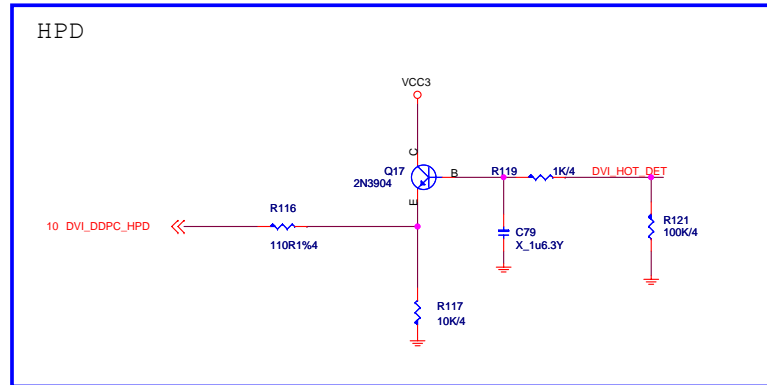
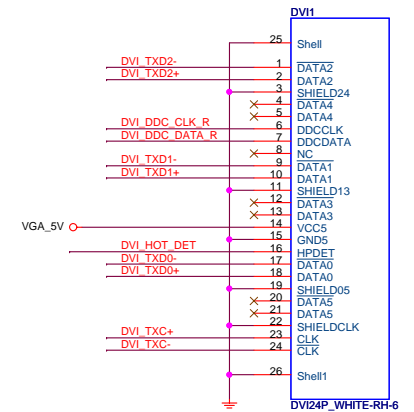
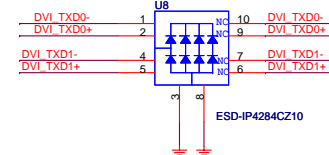
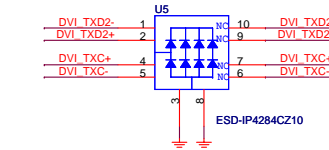
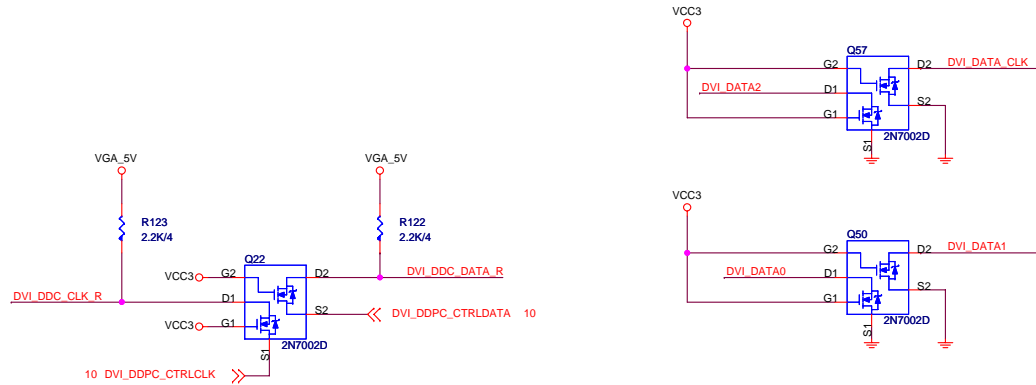


FRONT USB PORT 10,11

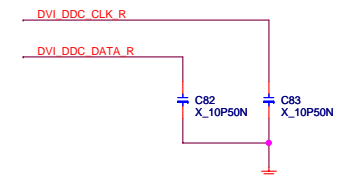
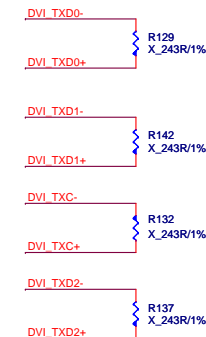


DVI level shifter

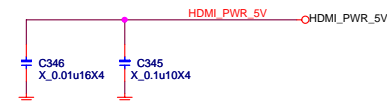
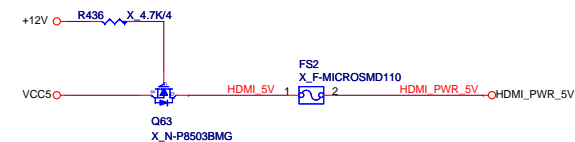
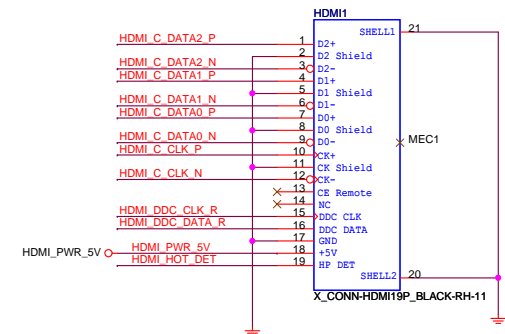
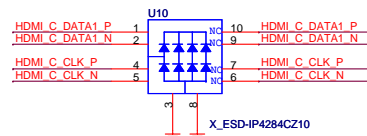
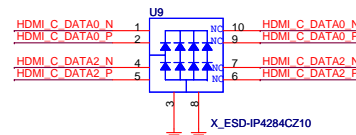
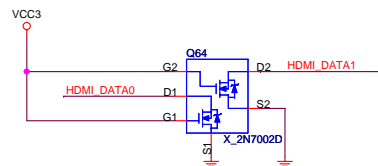
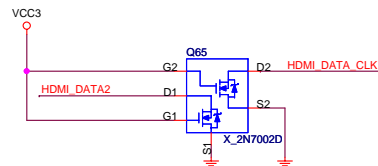
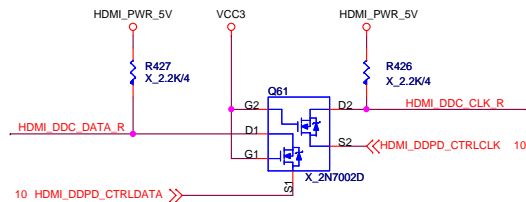
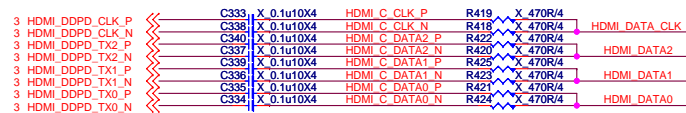
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



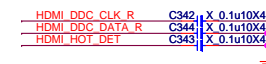
For EMI



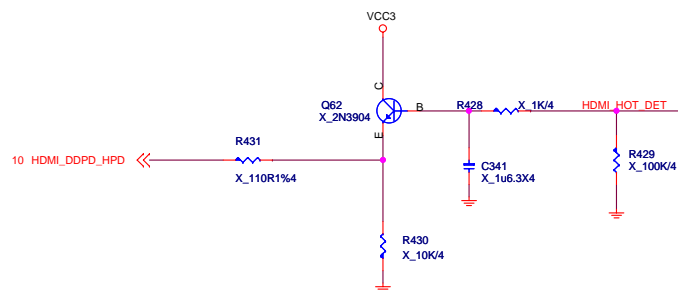
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



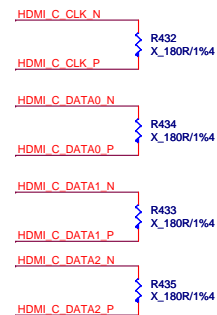
EMI



HPD



For EMI



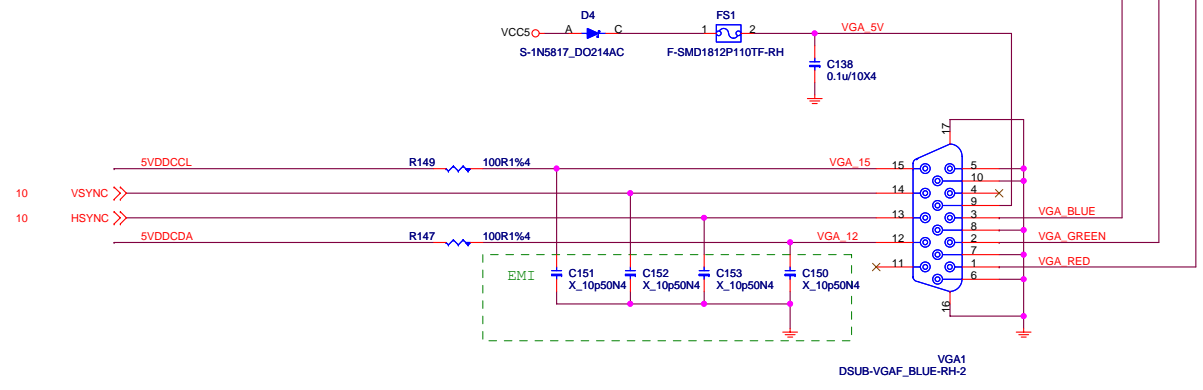
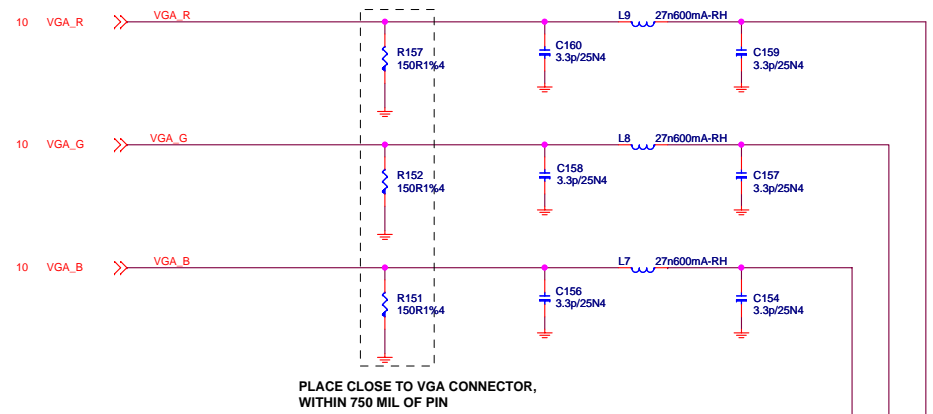
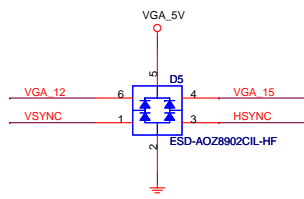
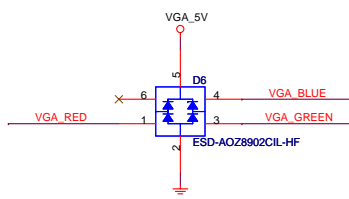
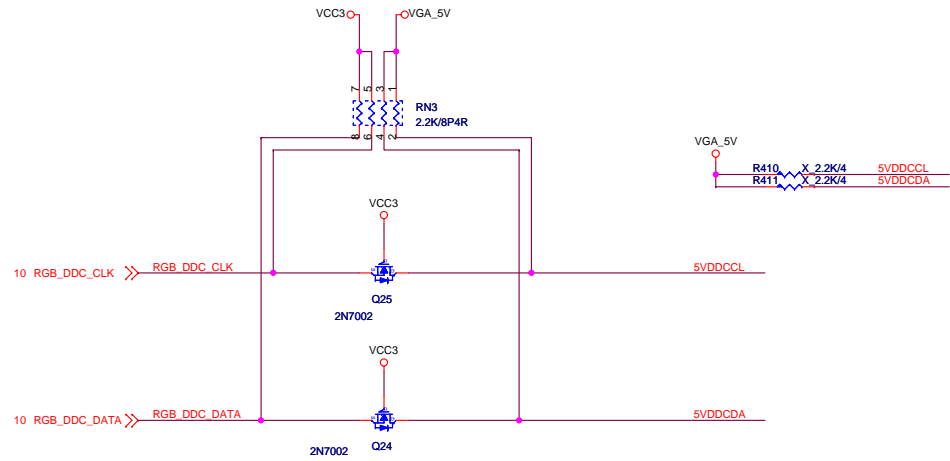
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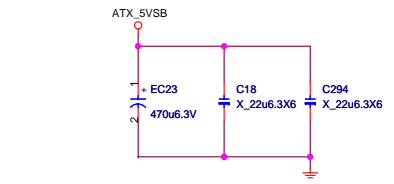
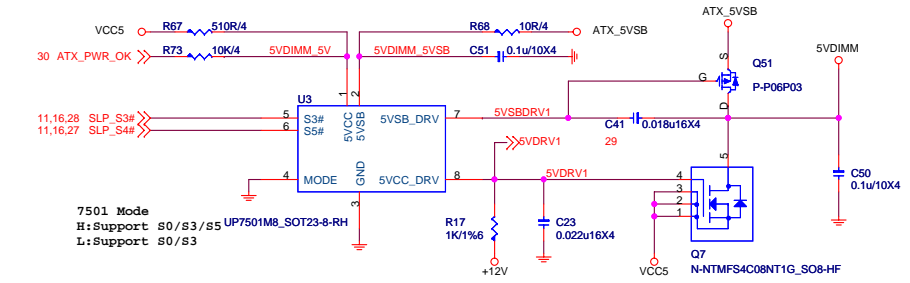
| Size | Document Description | Rev |
|-------------------------------|----------------------|-----|
| Custom | HDMI Connector | 12 |
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D-Sub

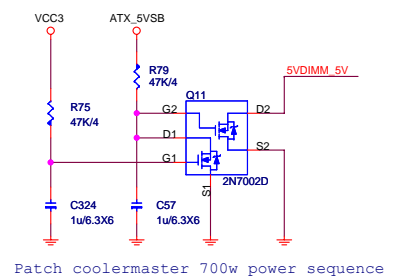
Level shift



5VDIMM FOR DDR

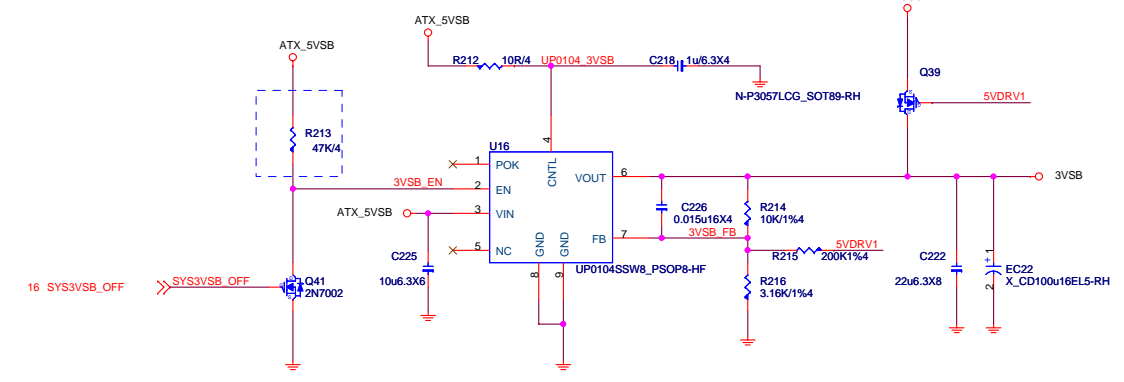


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



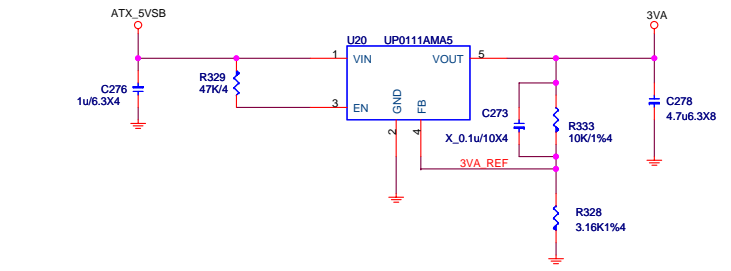
3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



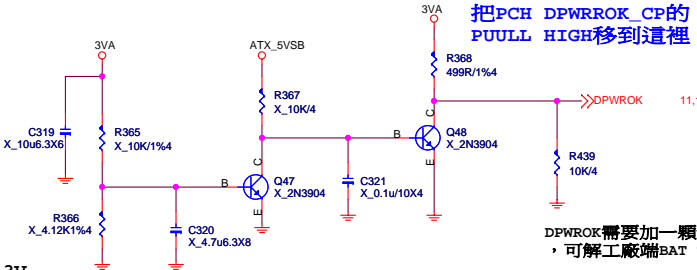
3VA

20mA



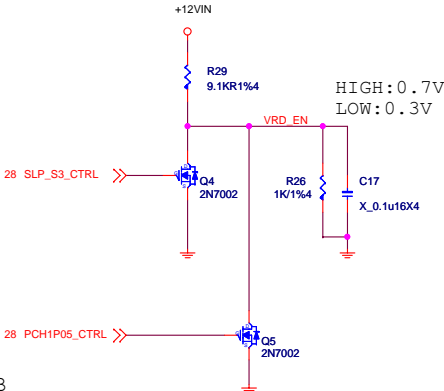
3.389V分壓=0.813V
2.71V分壓=0.65V

FOR DPWRK跟3VA的POWER
DOWN的時序(S5-->G3)



DPWRK需要加一顆pull down 10k電阻
，可解工廠端BAT 電流過大問題

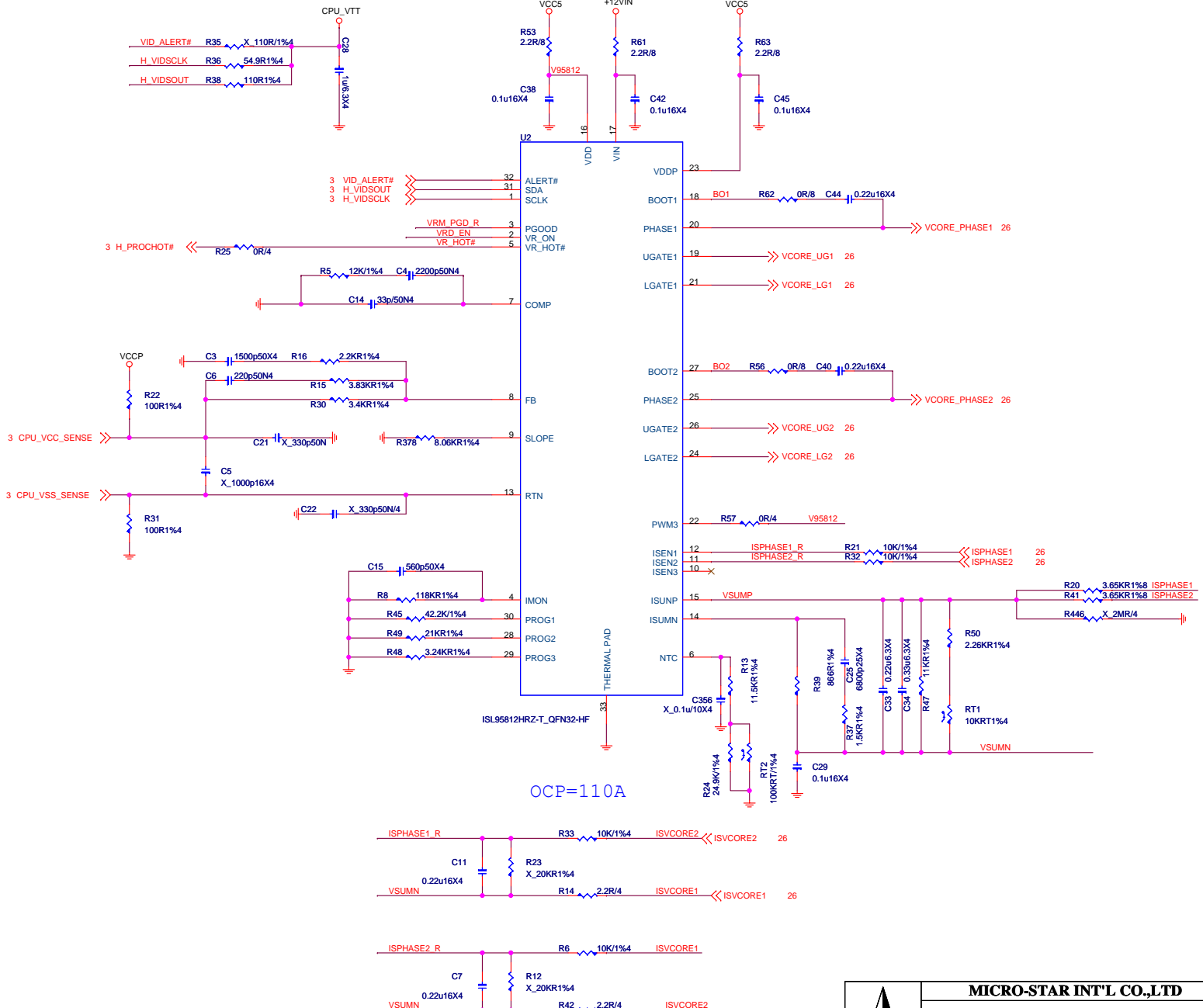
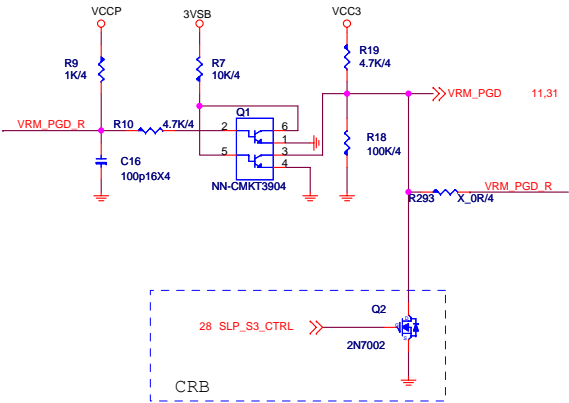
VCORE power on by s3 and 12v



CRB

HIGH:by PCH_1P05V
LOW:by S3

VRMPWRGD LEVEL SHIFT



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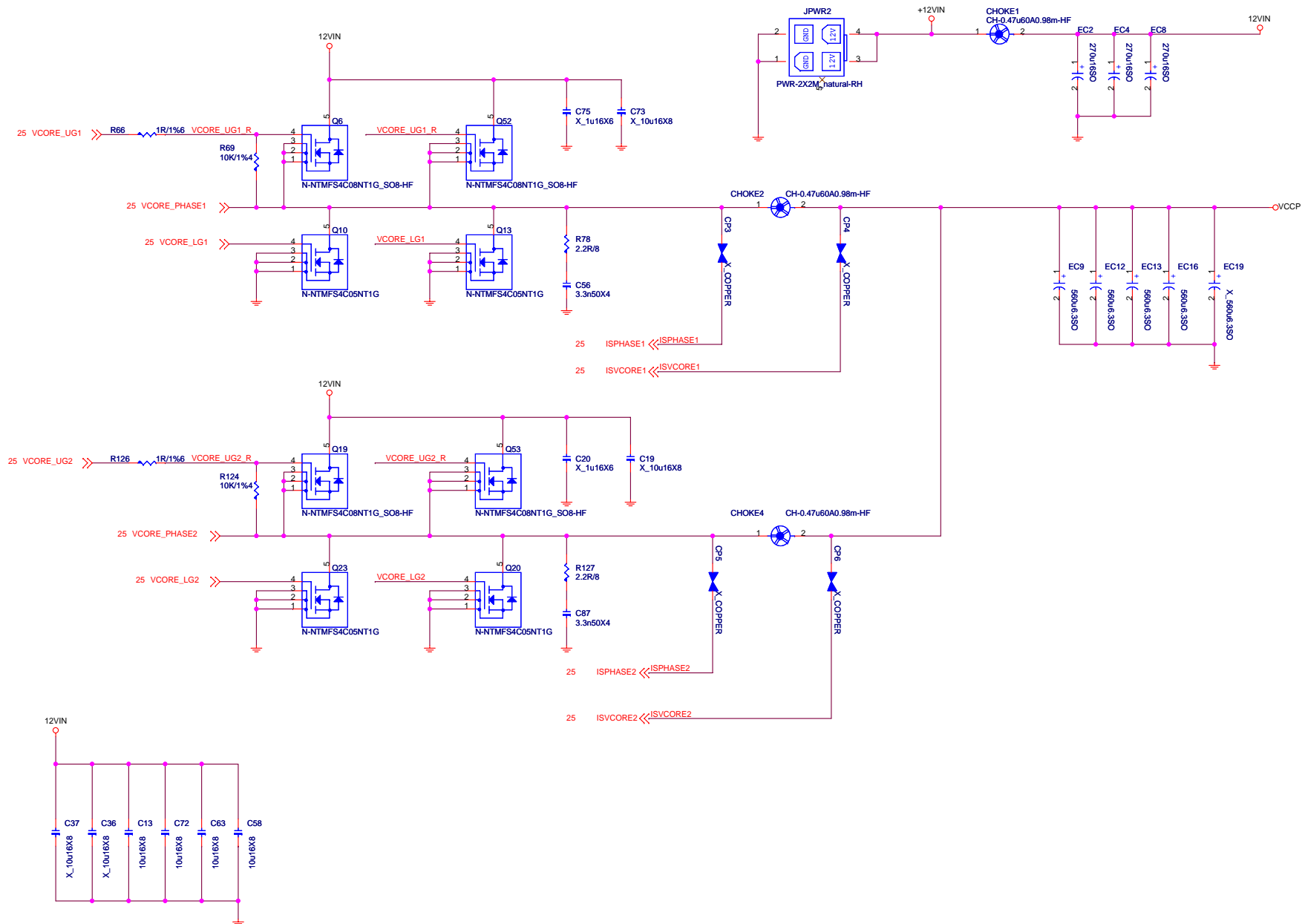
| |
|--------|
| Size |
| Custom |

Document Description
VRD12.5 - ISI.95818Rev
12

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|-------------------------------|----------------|
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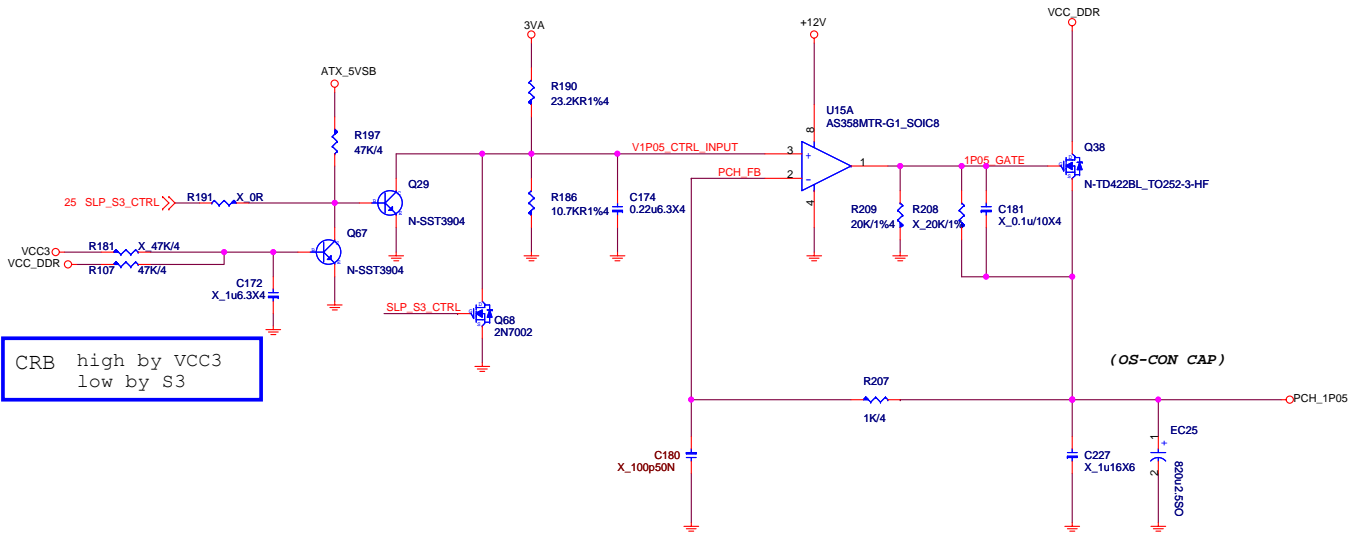
VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W
LL:2.5m ohm



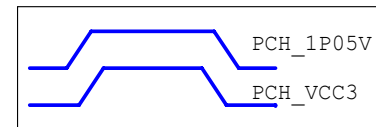
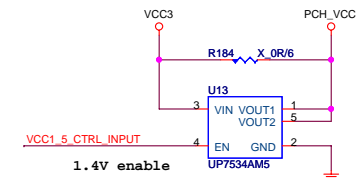
P.S. Only for meet Intel power down sequence.

PCH Power:1.05V 5.747A

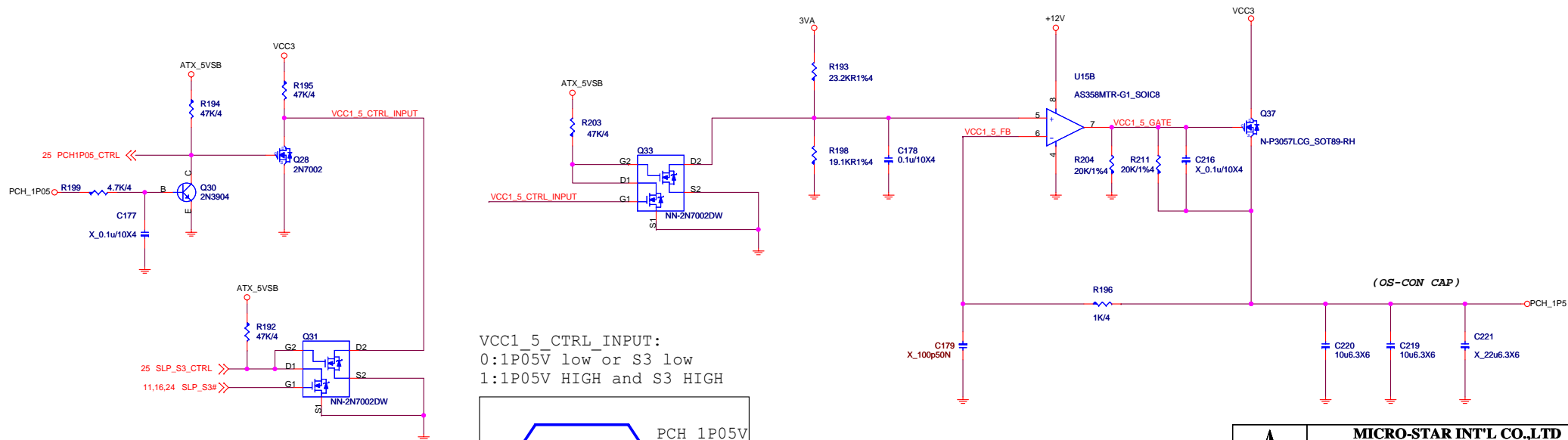


CRB high by VCC3
low by S3

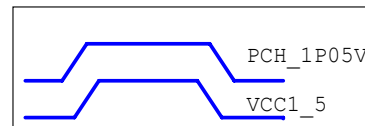
0.133A



PCH Power:1.5V 0.183A



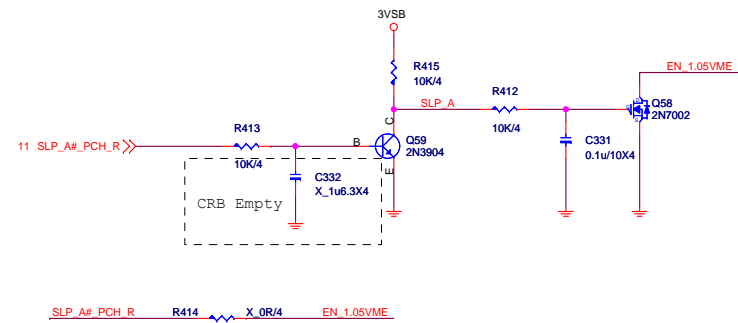
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



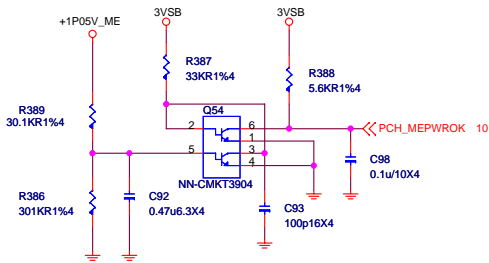
| MICRO-STAR INT'L CO.,LTD | | |
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| Size | Document Description | Rev |
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SLP_A

ME Power Control



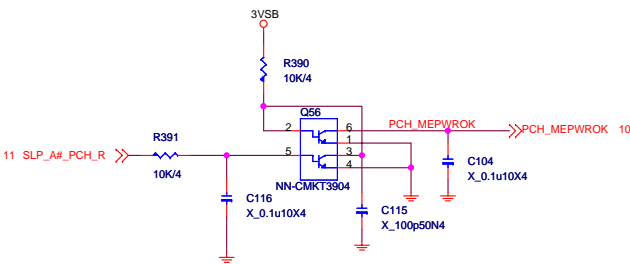
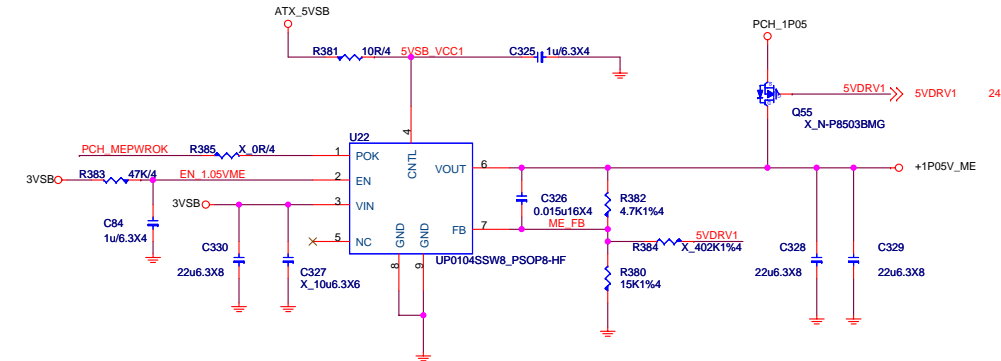
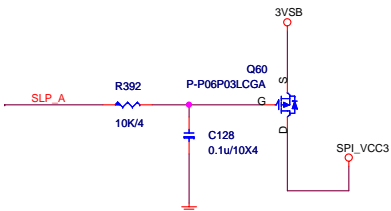
PCH_MEPWROK



VccASW active to APWROK high lms

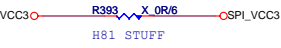
+3.3V_ME

+3.3V_ME



APWROK falling to VccASW falling 40ns

For INTEL ME

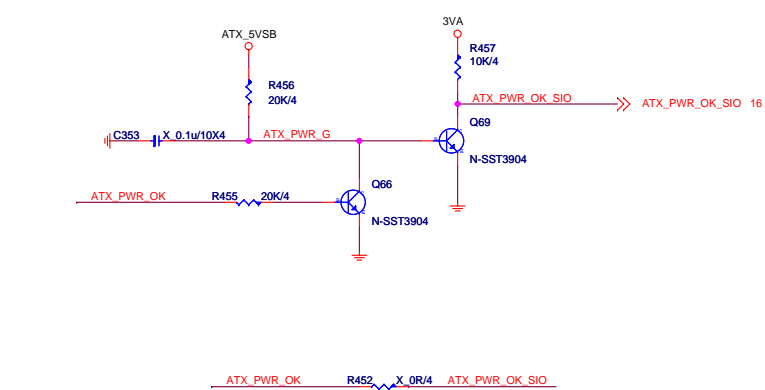
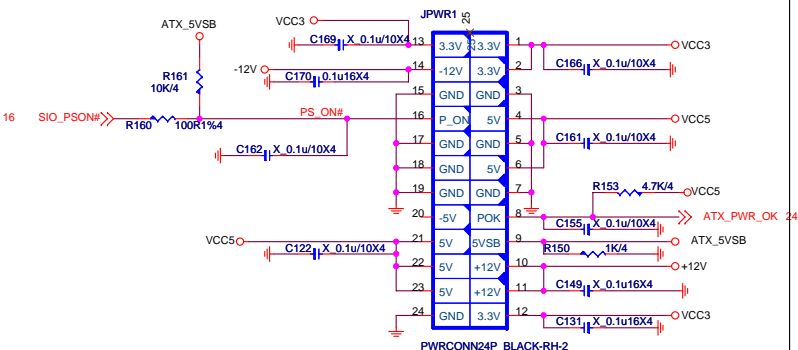


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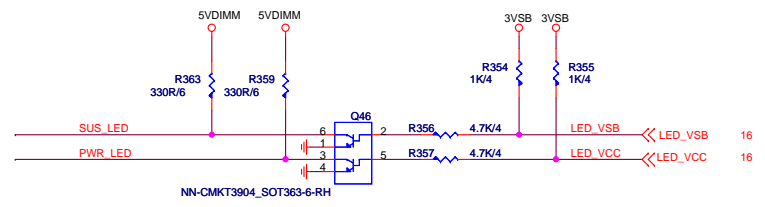
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| Custom | PCH Power - OP+MOS | 12 |
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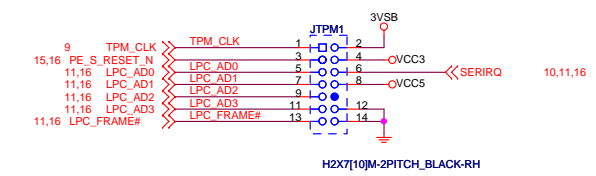
ATX POWER CONNECTOR



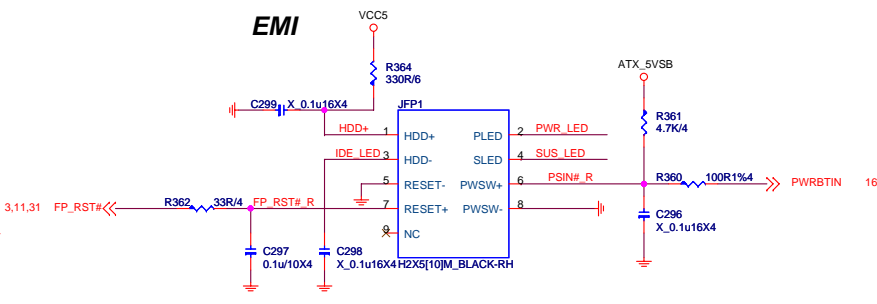
LED (for NV5533)



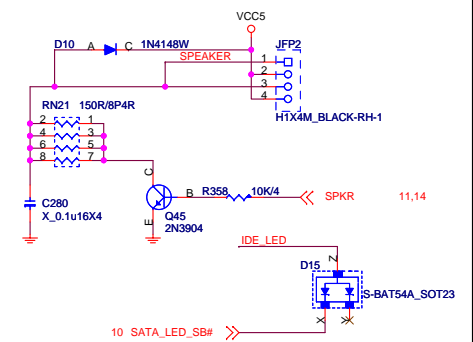
TPM/JLPC



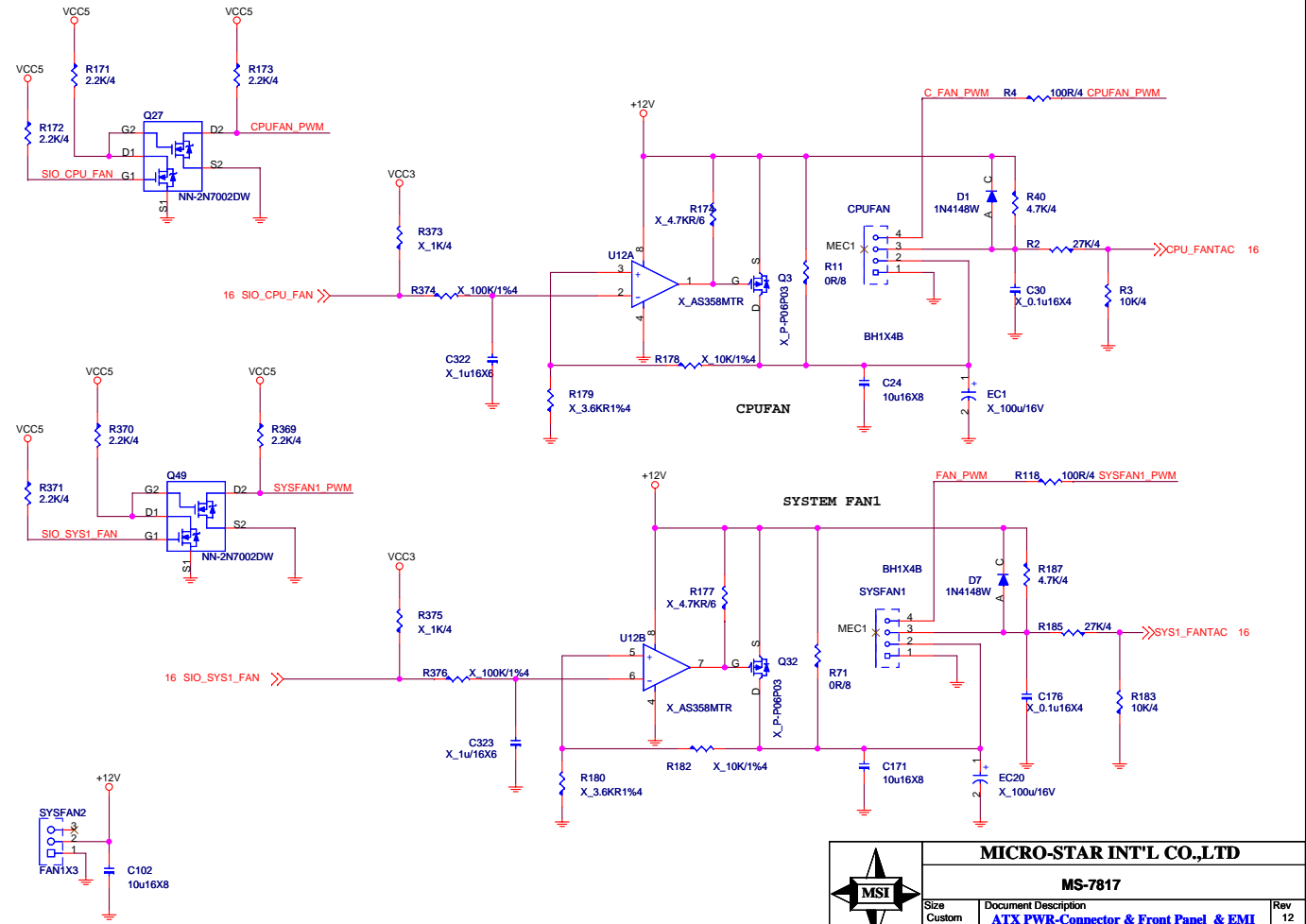
FRONT PANNEL



Speaker Pin Header



FAN-COUNTROL CIRCUIT

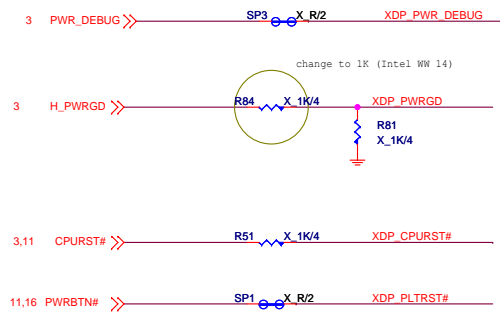
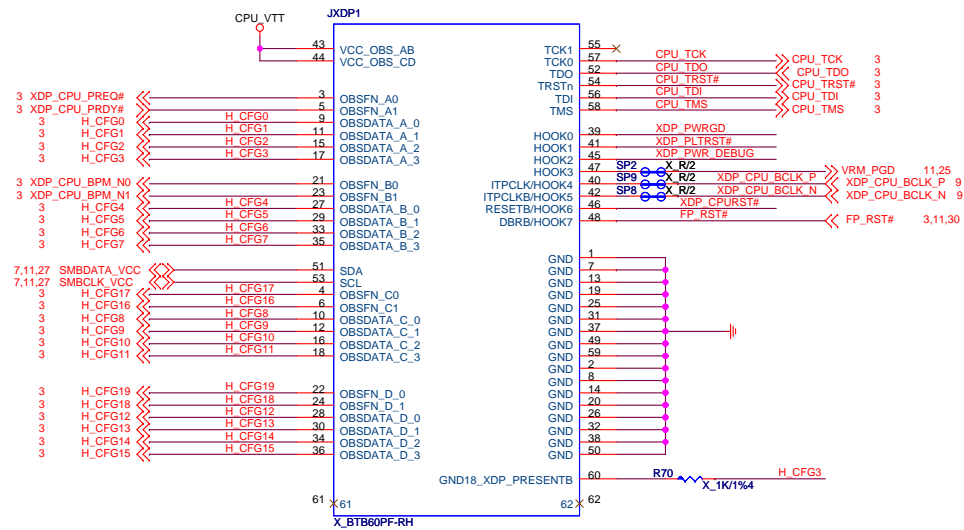


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Reserve debug port 5020



CPU TDO R96 X 51R/4 PCH_1P05

PLACE NEAR XDP CONNECTOR

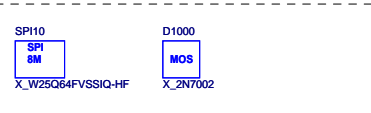


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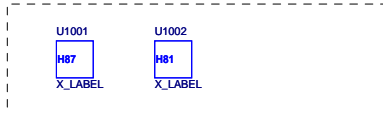
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|-------------------------------|--|----------------|
| Size Custom | Document Description XDP CPU & PCH | Rev 12 |
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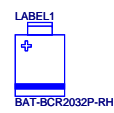
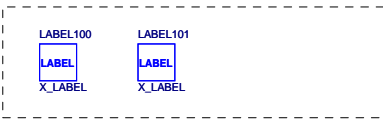
SPI OPT.



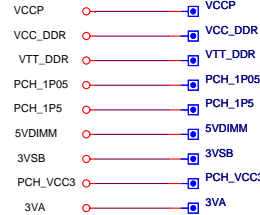
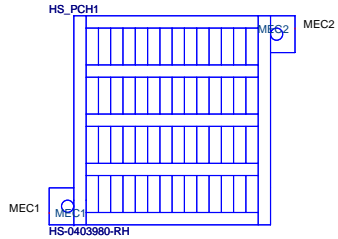
CHIPSET OPT.



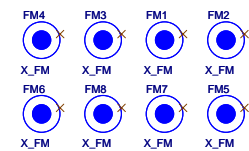
LABEL OPT.



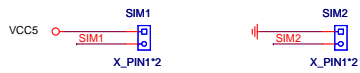
PCH XDP PWRGD/RESET



Optical Fiducial Marks-120



Simulation



Mounting Holes

